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A ring oscillator based on HIFETs

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ABSTRACT

A hygroscopic insulator field-effect transistor (HIFET) ring oscillator with three inverters was built and tested under ambient laboratory conditions. An operating voltage of −2 V was used, yielding a peak-to-peak output voltage of 1.1 V and an oscillation frequency of 28 mHz. For Spice (simulation program with integrated circuit emphasis) simulation of the HIFET circuits the measured HIFET output characteristics were fitted to a DC (direct current) model and additional measurements were made to find the magnitude of the capacitive and resistive elements in the HIFET gate structure. The results indicated that HIFETs have a good potential for use in amplifier and sensor circuit applications where high operation speed is not crucial.

1. Introduction

One of the most attractive properties of organic electronics is the possibility of using mass production methods, such as printing, to produce low-cost large-area electronic circuits and devices on flexible substrates. This requires the fabrication of high performance solution-processable polymer transistors [1]. Solution deposition of a multilayer transistor structure is challenging, especially at the active semiconductor/dielectric interface, where dissolution of the underlying layer may cause interfacial effects such as increased surface roughness which may have a disadvantageous effect on the electrical performance of the transistor [1]. The gate dielectric plays an important role in determining the properties of field-effect transistors, as the gate affects the transistor channel by means of electrostatic coupling, so that operation of the transistor at low voltages requires the use of a high permittivity dielectric or a very thin dielectric layer. Very thin polymer dielectric layers that are of high quality and free of pin-holes are difficult to fabricate by solution processing, and most polymers are of low permittivity. Hence, polymer transistors typically require high operating voltages (tens of volts).

Low-voltage operation of an organic transistor can alternatively be achieved with electrochemical transistors [2] or by using an electrolyte as a gate insulator [3,4]. Inverter and ring oscillator circuits with operation frequencies of $\sim 10^2$ Hz have been proposed for electrolyte-gated transistors [4,5]. The hygroscopic insulator field-effect transistor (HIFET) takes advantage of the fact that poly(4-vinylphenol) (PVP) is a weak electrolyte in contact with water, methanol or ethanol, and the operating principle differs from that of traditional organic field-effect transistors (OFETs) in that channel current modulation is not controlled by a pure field effect but is caused by H+ ions moving vertically in the hygroscopic insulator, where they build up opposite charge densities on the two sides of the insulator [6,7]. It has been proposed that the ions moving in the insulator may cause electrochemical oxidation and reduction of poly(3-hexylthiophene) (P3HT) at the P3HT/PVP interface, which results in modulation of the channel

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current of the transistor [6–8]. HIFETs have many advantageous properties, such as insensitivity to surface roughness [9] or insulator layer thickness [7]. A clear saturation region for transistor operation and relatively high channel current levels (a few μA's) are achievable at low operating voltages (less than 2 V). In addition, HIFETs have been fabricated completely on plastic substrates by printing methods [10]. Because of the current modulation mechanism, the internal operation of a HIFET is relatively slow [7], but there are many applications for which slow transistors are suitable, e.g. the measuring of long time intervals or use in conjunction with chemical sensors.

Effective design of organic transistor circuits requires a proper simulation model for the organic transistors. Various drain current models for OFETs have been presented, and a generic model has been developed for OFETs, which have many unique properties compared with traditional field-effect transistors (FETs) [11]. On the other hand, modified metal oxide semiconductor field-effect transistor (MOSFET) models are often used for OFETs, because of the many similarities in their characteristics [12], and the suitability of an amorphous silicon thin-film transistor (a-Si:H TFT) model [13] for organic transistors has also been demonstrated [14,15]. One advantage of the a-Si:H TFT model is that it includes gate bias-dependent mobility, which is also a typical feature of OFETs [16]. The above mentioned FET models can also be used with modified parameters for modeling the DC operation of a HIFET, because the current/voltage (I/V) characteristics of a HIFET are very similar in shape to typical field-effect transistor curves. The operating principle of a HIFET means that there is no straightforward physical basis for the model, so that the proper parameter values mainly have to be found by experimental adjustment.

We present here the operation principle and structure of a HIFET ring oscillator consisting of three inverter stages, and quote some measurement results. A physically simplified Spice model has also been developed for the simulation of HIFET circuits.

2. Experimental

A typical structure for a top-gate, bottom-contact HIFET is shown in Fig. 1a. HIFETs with two channel widths (W = 1.5 and 7.5 mm) but the same channel length (L = 25 μm) were fabricated on laboratory glass slides and subjected to ultrasonication at 60 °C in H_2O, acetone and isopropanol for 10 min each. Gold electrodes around 30 nm thick were then vacuum-evaporated onto the substrates through a shadow mask, and a roughly 50 nm thick semiconducting layer was fabricated on the substrates by spin-casting P3HT (Plextronics) from an 8 mg/ml solution in p-xylene. The samples were dried at 70 °C for 20 min before the ~1 μm thick PVP (Sigma–Aldrich) dielectric layer was spin-cast from a 100 mg/ml solution in ethyl acetate. The chemical structures of P3HT and PVP are presented in Fig. 1b and c, respectively. Pedot:PSS (Poly(3,4-ethylenedioxythiophene):poly(styrene sulphonate)) (Baytron-P, from H.C. Starck) gate electrodes were fabricated manually after the dielectric film had dried for 30 min at 70 °C.

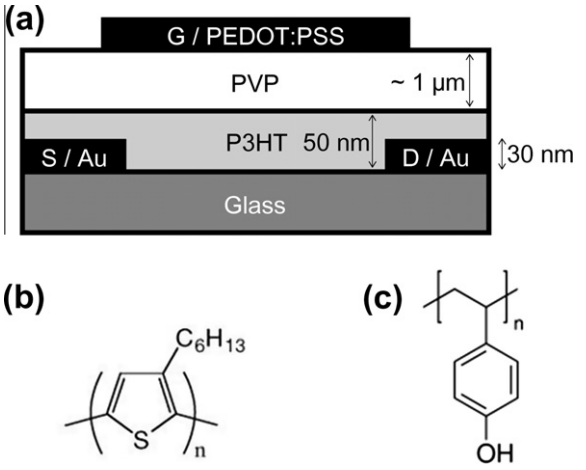

Fig. 1. (a) Schematic cross-section of a HIFET structure and the chemical structures of (b) the P3HT semiconductor and (c) the PVP insulator.

The oscillator circuit was built using PCB (printed circuit board) wiring and discrete HIFETs on glass slides that were fastened to the PCB with double-sided tape. The electrical contacts with the PCB were made with screw connectors and the wires were glued to the electrodes of the transistors with electrically conductive paint (ELEKTROLUBE® SCP). The ring oscillator was composed of three inverters (of the design presented in Fig. 2) connected in a loop. Because of the asymmetry of the voltage transfer characteristics of simple HIFET enhancement load inverters, referred to here as amplifier stages, they could not be used to drive subsequent inverters while sustaining logic integrity [17]. Consequently a level shifter was added to make the inverter characteristic more symmetrical.

The curves for the characteristics of the HIFETs and inverters were measured with a Keithley 4200-SCS semiconductor parameter analyzer using a scan speed of 0.1 Vs^{-1}. The output voltage of the oscillator and the voltages in the circuit nodes during the electrical testing

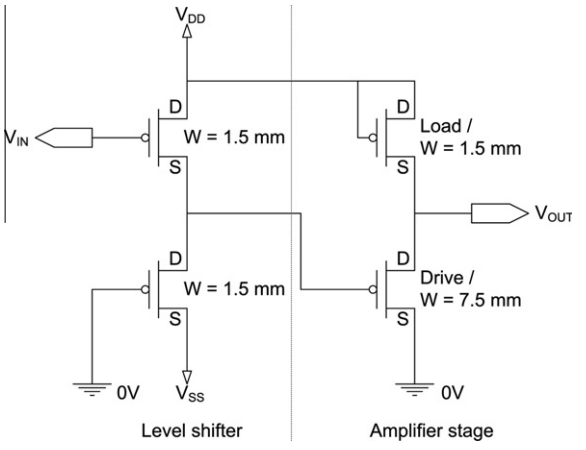

Fig. 2. Schematic diagram of the circuit of the HIFET inverter.

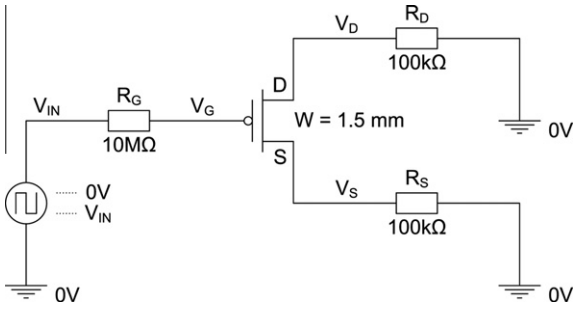

Fig. 3. The circuit used in the experiment to examine HIFET gate currents. The currents at the transistor terminals were determined by measuring the voltage drop across the resistors R_G, R_D and R_S when using a square wave input voltage (V_{IN}).

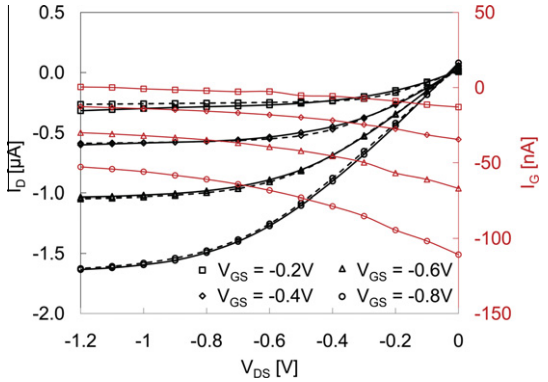

Fig. 4. Measured (solid line) and simulated (dashed line) output characteristics and the gate currents (red solid line) of a HIFET (W = 1.5 mm and L = 25 μm). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

of the HIFETs were measured with an oscilloscope using high input impedance, a low bias current and low offset voltage operational amplifiers as voltage buffers.

The HIFETs typically have fairly high gate currents and this should be taken into account in the simulation of HIFET circuits. It has been suggested that the gate currents of a HIFET can be attributed both to electronic leakage currents and to the drift of ionic species [8]. We consider the nature of electronic leakage currents to be resistive, ionic drift currents are mostly capacitive in nature, because they are related to the formation of a double layer capacitance. However, if ions can diffuse into the semiconductor or gate material, the effect could also be both resistive and capacitive. An additional capacitive contribution to the gate current is received from electronic capacitance charge currents arising from stray capacitances in the gate. When modeling the dynamic operation of a transistor the capacitances in its structure must be included in the simulation. An experimental method was used here to find the magnitude of the capacitive and resistive elements in the HIFET gate structure. The circuit used in the experiment is presented in Fig. 3. The gate (I_G), drain (I_D) and source (I_S) currents were calculated by measuring the voltage drop across 100 kΩ resistors at the drain and source and a 10 MΩ resistor at the gate when a square wave voltage pulse was used at the input (V_{IN}). The input (V_{IN}), gate (V_G), drain (V_D) and source (V_S) voltages were measured with an oscilloscope (voltage buffer gain was 1 for gate voltage and 100 for drain and source voltages). Measurements were performed at five amplitudes of the square wave pulse.

The HIFETs were handled throughout the tests in a normal laboratory atmosphere and at constant humidity (RH ~43%), the latter being maintained with an aqueous solution of potassium carbonate. It is typical for the current modulation in a HIFET to improve in the presence of excess air humidity in terms of both water and ethanol [7].

3. Results and discussion

3.1. HIFET and oscillator measurements

Typical output characteristic curves together with the gate currents of a smaller (load) transistor are presented in Fig. 4. The magnitude of the drain currents of the larger (drive) transistors scaled approximately with the dimensions, and the shapes of the characteristic curves were similar. Due to variation in the threshold voltage (V_t) and transconductance (g_m) values, the transistors were not completely uniform in their characteristics and the current levels did not scale exactly with their dimensions. A voltage gain ($Av = -\sqrt{((W/L)_{driver}/(W/L)_{load})}$) [18] of ~2.2 was achieved using a single amplifier stage with a driver transistor that was five times wider than the load transistor.

Measured voltage transfer characteristics of the whole inverter stage at three bias voltages (V_{SS}) are presented in Fig. 5. A rise time ($t_{r(10-90\%)}$) of 10.4 s was measured for the output voltage of the inverter when a square wave voltage signal of −0.8 ± 0.05 V was used in the input. Since the channel currents through the transistors varied roughly between 1 and 10 μA during operation of the oscillator, the measured gate leakage currents, with magnitudes of ~1 –100 nA, slightly reduced the total gain of the oscillator. There is a possibility that some of the gate

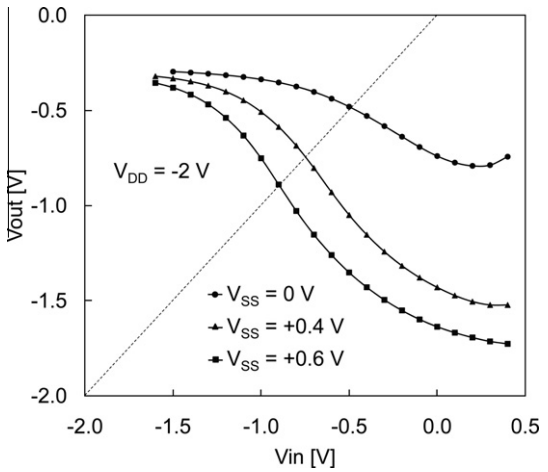

Fig. 5. Voltage transfer characteristics of the HIFET inverter at three values of V_{SS}.

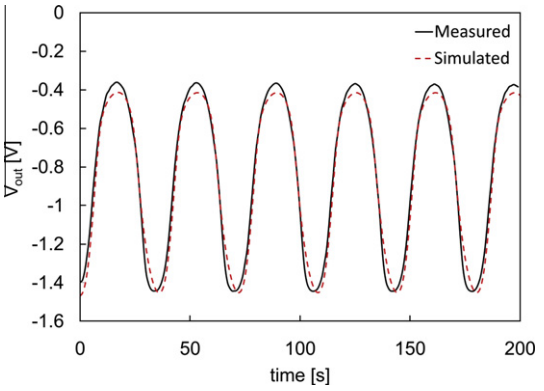

Fig. 6. Measured and simulated output voltage of the HIFET oscillator.

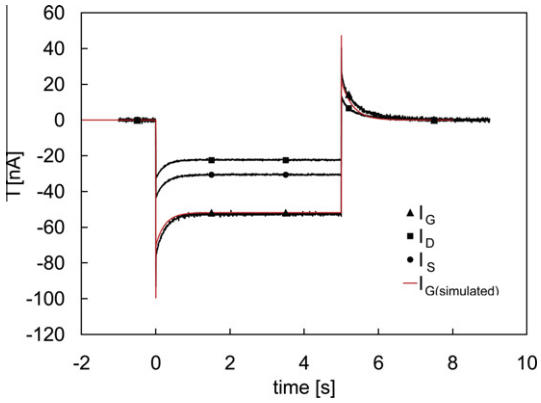

Fig. 7. Measured currents at the transistor terminals in an experiment to examine the gate structure of a HIFET. Test circuit input voltage V_{IN} was −1 V. The simulated gate current is also depicted in the figure.

leakage can be attributed to water electrolysis, since the HIFETs are operated above the threshold of dissociation for water (1.2 V at PH = 7) and minor degradation is observed. PVP is a weak electrolyte, however, and the effect seems to be small. Another effect is that the gate leakage could result from the non-ideal insulator (resistive) properties of the wet PVP dielectric. Individual values for the bias voltage V_{SS} had to be used in the separate level shifter stages of the inverters in the oscillator circuit due to variations in the transistor parameters.

The output voltage signal of the oscillator is presented in Fig. 6. The peak-to-peak value of the measured output voltage and oscillating frequency were 1.1 V and 28 mHz, respectively. The operating voltage V_{DD} was −2 V, and the bias voltages V_{SS} of individual amplifier stages were +0.7, +0.7 V and +0.94 V.

3.2. Modeling and simulation of a HIFET

We used a-Si:H TFT model [14] with modified parameter values as a DC model for a HIFET. The simulated output characteristics of a HIFET are also depicted in Fig. 4, and show a reasonably good match with DC operation. The a-Si:H TFT model describes the transistor drain current in the linear and saturation regions with a single equation. The equation and related parameters are presented in Ref. [14]. It is not reasonable to model HIFET currents in the sub-threshold region because sub-threshold operation of a HIFET is obscured by the gate leakage currents.

The currents measured at the transistor terminals when a square wave (V_{IN}) of amplitude −1 V and pulse length 5s was used in the test circuit presented in Fig. 3 is shown in Fig. 7. The resistive (DC) parts of the leakage currents were calculated from the stabilized parts of the pulses and the capacitances from gate to drain and source were calculated from the time-varying part of the current pulses (see Fig. 7).

The stabilized currents measured at the transistor terminals are not linear functions of the gate voltage, as would probably be the case if only an electronic leakage current existed. Instead the stabilized current depends on the second power of the gate voltage, indicating that the current not only represents electrical leakage but is also affected by another mechanism such as water electrolysis or ion diffusion. One explanation can also be that part of the resistances R_{GS} and R_{GD} originate from the channel resistance R_{SD}, which in a normal FET has a second power dependence on the V_{GS}. The leakage current from the gate to the drain can be approximately represented as a function of V_{GD} with an experimental equation such as:

$$I_{GD} = -6.14 \times 10^{-8} \times (|V_{GD}|)^2 + \frac{V_{GD}}{50.9\text{M}\Omega}, \quad (1)$$

and the current from the gate to the source can be presented as a function of V_{GS} as:

$$I_{GS} = -5.06 \times 10^{-8} * (|V_{GS}|)^2 + \frac{V_{GS}}{26.8\text{M}\Omega}. \quad (2)$$

The formulas [1] and [2] differ because of the unintentional asymmetry of the transistor under examination. The non-linear resistors R_{GS} and R_{GD} have been added to the simulation model (Fig. 8) in the form of a voltage-dependent current source, according to the above equations.

It was also noticed that two additional capacitances and a resistor are needed in both GS and GD circuits to model the measured values shown in Fig. 7. The serial connections R1-C1 and R2-C2 model the varying part of the current pulse, and the spikes measured in the current pulse indicate that there is also a relatively small capacitance parallel with the resistor which shorts the resistor at high frequencies. We have attributed the varying part of the current pulse to ion drift in the moist PVP and the formation of the double layer capacitances at the two interfaces with the PVP, including the parasitic capacitances in the gate. The proper values for these capacitors and the resistor were found by simulating the circuit used in the measurements and adjusting the values so that the simulation matched the measured results. The simulated gate current matched well with the measurements, as can be seen in Fig. 7.

The simulation model for a HIFET was completed by combining the DC model with the gate model developed here, as presented in Fig. 8. Simulation of the ring oscillator using the developed model indicates that the capacitances related to the transistor gate structure do not explain thoroughly the slow operation of HIFET. Indeed, using the input node of the transistor as the effective input node of the gate,

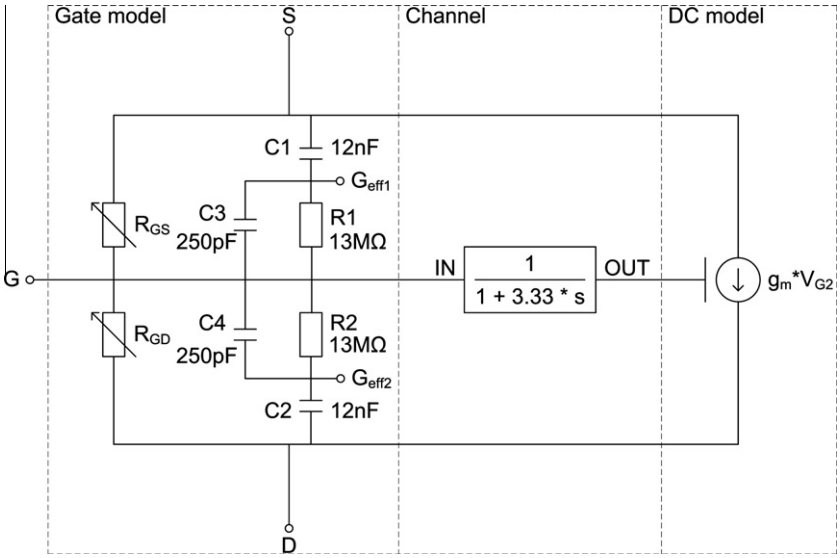

Figure 8. Simplified HIFET simulation model.

the oscillator circuit reached in the simulator a frequency of about 800 Hz, which is a much higher value than the measured one. If we attribute C1 (or C2) to the double layer capacitance and use the connection between C1 and R1 (or C2/R2) as the gate input (named G_{eff1} and G_{eff2} in Fig. 8), simulation gives an oscillation frequency of 500 mHz. It seems that in the HIFET device there exists still a slower process, which controls the channel current modulation. In the simulation model developed here this operational slowness is modeled simply by adding a single pole low pass filter to the gate model, as presented in Fig. 8. One option for explaining the additional slowness is an interfacial electrochemical oxidation/reduction process in the semiconductor [6–8], which sets a time constant and limit for the HIFET operation speed. The slow channel current response may partly be also due to the parasitic capacitances and resistances, exerting an external load on the transistor channel, because the functional layers of the HIFETs were not exactly patterned and the structural dimensions were not minimized for optimal transistor performance. Use of a low pass filter with a time constant τ of 3.33 s gave a simulated oscillator frequency which is comparable to the measured one, as presented in Fig. 6. In practice the model developed here gave reasonably good results in the simulation of HIFETs. It must be pointed out that the operation of the HIFET is not purely FET-like and further examination for the nature of the oxidation/reduction process is needed, also for developing the electrical model to a more detailed one.

4. Conclusions

The 3-stage HIFET ring oscillator presented here achieved an output voltage of 1.1 V and an oscillating frequency of 28 mHz with an operating voltage of −2 V. A reasonably good match with the measured results was observed in Spice simulation when a modified a-Si:H TFT model was used as a DC model for the HIFETs. To simulate the dynamic operation of a HIFET circuit the capacitances and resistances in the gate structure were extracted by means of experimental measurements and added to the simulation model. The simulation suggests that the operating speed of an HIFET is not limited by the capacitance but instead the operational slowness is possibly related to an electrochemical doping process, that could control the current modulation in a HIFET. The low operating voltage makes HIFETs attractive components for practical applications despite this operational slowness.

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